What is claimed is:

1. A method for programming a p-channel MOSFET in a substrate into a reprogrammable switch, the method comprising:

applying a first voltage potential to a source region of the MOSFET;

applying a second voltage potential to a drain region of the MOSFET; and

applying a negative gate potential to a gate region of the MOSFET,

wherein applying the first and second voltage potentials and the negative gate potential causes a hot hole injection from the substrate into a gate oxide of the MOSFET.

2. The method of claim 1, wherein applying the first voltage potential to the source region of the MOSFET comprises grounding the source region of the MOSFET.

3. The method of claim 1, wherein applying the second voltage potential to the drain region of the MOSFET comprises grounding the drain region of the MOSFET.

4. The method of claim 1, wherein applying the negative gate potential to the gate region of the MOSFET comprises applying a sufficiently large negative gate potential to form a conduction channel between the source and drain regions of the MOSFET.

5. The method of claim 1, further comprising operating the MOSFET in a forward direction in a programmed state by:

coupling a sourceline to the source region;

coupling a bitline to the drain region; and

applying a gate potential to the gate region such that a conduction channel is formed between the source region and the drain region.

6. A method for programming a p-channel MOSFET in a substrate into a reprogrammable switch, the method comprising:

coupling a source region of the MOSFET and a drain region of the MOSFET to an electrical ground; and

applying a negative gate potential to a gate region of the MOSFET,

wherein applying the negative gate potential to the gate region causes a hot hole injection from the substrate into a gate oxide of the MOSFET.

7. A method for performing address decoding in a memory, the method comprising:

coupling a plurality of address lines and a plurality of output lines to a programmable decoder having a plurality of rows and a plurality of redundant rows; and

unselecting a row by using hot hole injection to program a programmable switch associated with the row, the programmable switch comprising a metal oxide semiconductor field effect transistor (MOSFET) in a substrate, the MOSFET having a first source/drain region, a second source/drain region, a channel region between the first and second source/drain regions, and a gate separated from the channel region by a gate oxide,

wherein the MOSFET is a programmed MOSFET having a positive charge trapped in the gate oxide such that a threshold voltage of the MOSFET is significantly altered compared to a threshold voltage of the MOSFET in an unprogrammed state.

8. The method of claim 7, further comprising selecting a redundant row by reprogramming a programmable switch associated with the redundant row, the programmable switch comprising a metal oxide semiconductor field effect transistor (MOSFET) in a substrate, the MOSFET having a first source/drain region, a second source/drain region, a channel region between the first and second source/drain regions, and a gate separated from the channel region by a gate oxide, wherein the programmable switch associated with the redundant row is reprogrammed by removing a trapped

positive charge from the gate oxide.

9. The method of claim 7, wherein using hot hole injection to trap the positive charge in the gate oxide comprises:

applying a first voltage potential to a source region of the MOSFET;

applying a second voltage potential to a drain region of the MOSFET; and

applying a negative gate potential to a gate region of the MOSFET,

wherein applying the first and second voltage potentials and the negative gate potential causes a hot hole injection from the substrate into a gate oxide of the MOSFET.

10. The method of claim 9, wherein applying the first voltage potential to the source region of the MOSFET comprises grounding the source region of the MOSFET.

11. The method of claim 9, wherein applying the second voltage potential to the drain region of the MOSFET comprises grounding the drain region of the MOSFET.

12. The method of claim 9, wherein applying the negative gate potential to the gate region of the MOSFET comprises applying a sufficiently large negative gate potential to form a conduction channel between the source and drain regions of the MOSFET.

13. The method of claim 9, further comprising operating the MOSFET in a forward direction in a programmed state by:

coupling a sourceline to the source region;

coupling a bitline to the drain region; and

applying a gate potential to the gate region such that a conduction channel is formed between the source region and the drain region.

14. A method for programming an address decoder in a memory, the method comprising:

writing to a metal oxide semiconductor field effect transistor (MOSFET) associated with a row of the address decoder, thereby causing a positive charge to be trapped in a gate oxide of the MOSFET associated with the row, wherein writing to the MOSFET associated with the row causes the row to be uncoupled from a row driver; and

erasing a MOSFET associated with a redundant row of the address decoder, thereby removing a positive charge trapped in a gate oxide of the MOSFET associated with the redundant row, wherein erasing the MOSFET associated with the redundant row causes the redundant row to be coupled to a redundant row driver.

15. The method of claim 14, wherein writing to the MOSFET associated with the row of the address decoder comprises using hot hole injection to trap the positive charge in the gate oxide of the MOSFET associated with the row of the address decoder.

16. The method of claim 15, wherein using hot hole injection to trap the positive charge in the gate oxide of the MOSFET associated with the row of the address decoder comprises:

applying a first voltage potential to a source region of the MOSFET;

applying a second voltage potential to a drain region of the MOSFET; and

applying a negative gate potential to a gate region of the MOSFET,

wherein applying the first and second voltage potentials and the negative gate potential causes a hot hole injection from the substrate into a gate oxide of the MOSFET.

17. The method of claim 16, wherein applying the first voltage potential to the source region of the MOSFET comprises grounding the source region of the MOSFET.

18. The method of claim 16, wherein applying the second voltage potential to the drain region of the MOSFET comprises grounding the drain region of the MOSFET.

19. The method of claim 16, wherein applying the negative gate potential to the gate region of the MOSFET comprises applying a sufficiently large negative gate potential to form a conduction channel between the source and drain regions of the MOSFET.

20. The method of claim 16, further comprising operating the MOSFET in a forward direction in a programmed state by:

coupling a sourceline to the source region;

coupling a bitline to the drain region; and

applying a gate potential to the gate region such that a conduction channel is formed between the source region and the drain region.

21. The method of claim 14, wherein erasing the MOSFET associated with a redundant row of the address decoder comprises using reverse hot hole injection to remove the trapped positive charge from the gate oxide of the MOSFET associated with the redundant row of the address decoder.